1 KBit Read/Write Contactless Identification Device

Description

The EM4450 is a CMOS integrated circuit intended for use in electronic Read/Write RF Transponders. The chip contains 1K Bit of EEPROM which can be configured by the user, allowing a write inhibited area, a read protected area, and a read area output continuously at power on. The memory can be secured by using the 32 bit password for all write and read protected operations. The password can be updated, but never read. The fixed code serial number and device identification are laser programmed making every chip unique.

The EM4450 will transmit data to the transceiver by modulating the amplitude of the electromagnetic field, and receive data and commands in a similar way. Simple commands will enable to write EEPROM, to update the password, to read a specific memory area, and to reset the logic.

The coil of the tuned circuit is the only external component required, all remaining functions are integrated in the chip.

Features

- 1 K bit of EEPROM organized in 32 words of 32 bits
- 32 bit Device Serial Number (Read Only Laser ROM)
- 32 bit Device Identification (Read Only Laser ROM)
- Power-On-Reset sequence
- Power Check for EEPROM write operation
- User defined Read Memory Area at Power On
- User defined Write Inhibited Memory Area
- User defined Read Protected Memory Area
- Data Transmission performed by Amplitude Modulation
- Two Data Rate Options 2 KBd (Opt64) or 4 KBd (Opt32)
- Bit Period = 64 or 32 periods of field frequency
- 170pF ± 2% on chip Resonant Capacitor
- -40 to +85°C Temperature range
- 100 to 150 kHz Field Frequency range
- On chip Rectifier and Voltage Limiter
- No external supply buffer capacitance needed due to low power consumption
- Available in chip form for mass production and PCB and CID package for samples.

Applications

- Ticketing
- Automotive Immobilizer with rolling code
- High Security Hands Free Access Control
- Industrial automation with portable database
- Manufacturing automation
- Prepayment Devices
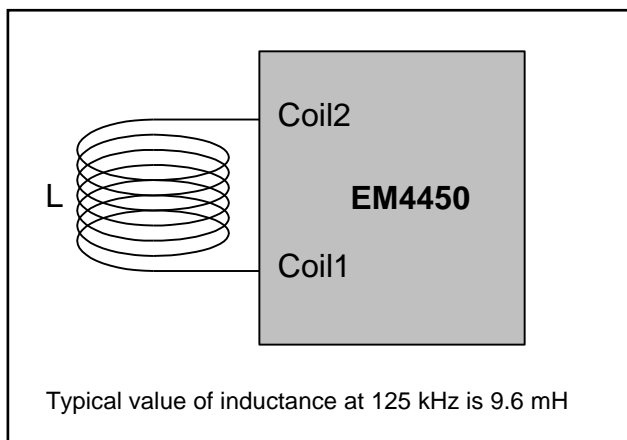
Typical Operating Configuration

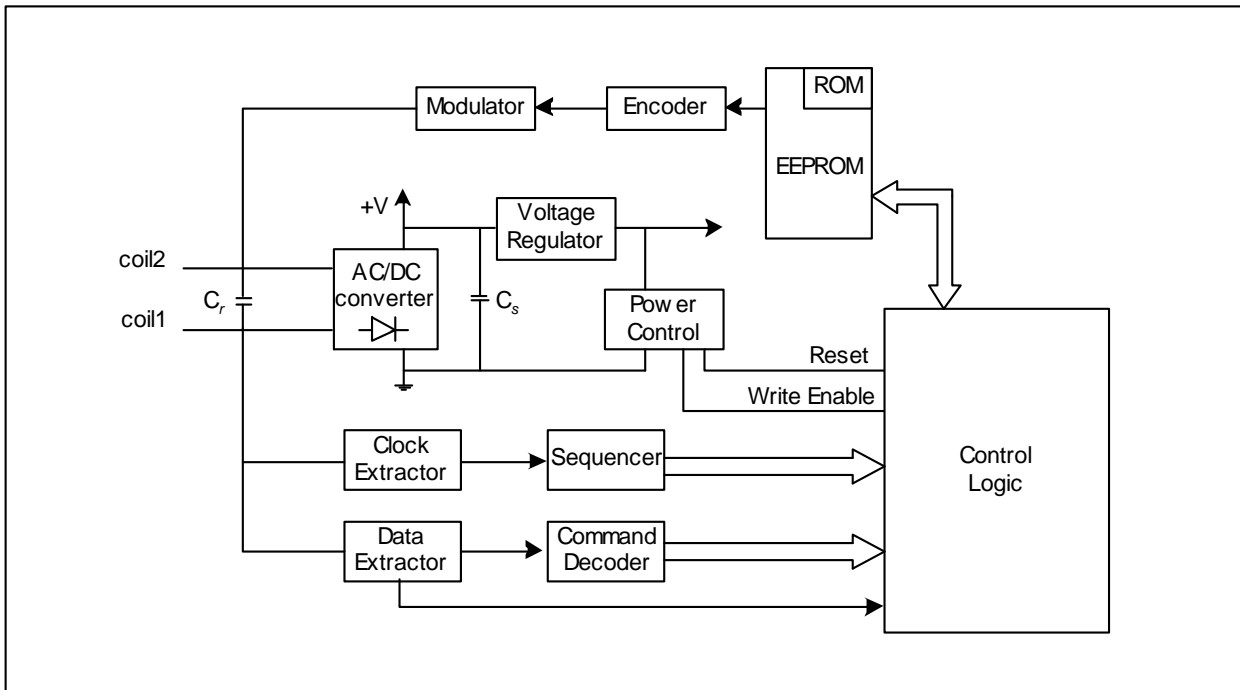Typical value of inductance at 125 kHz is 9.6 mH

Fig.1

www.emmicroelectronic.com

A COMPANY OF THE **SWATCH GROUP**

Block Diagram

Fig. 2

System Principle

Fig. 3

www.emmicroelectronic.com
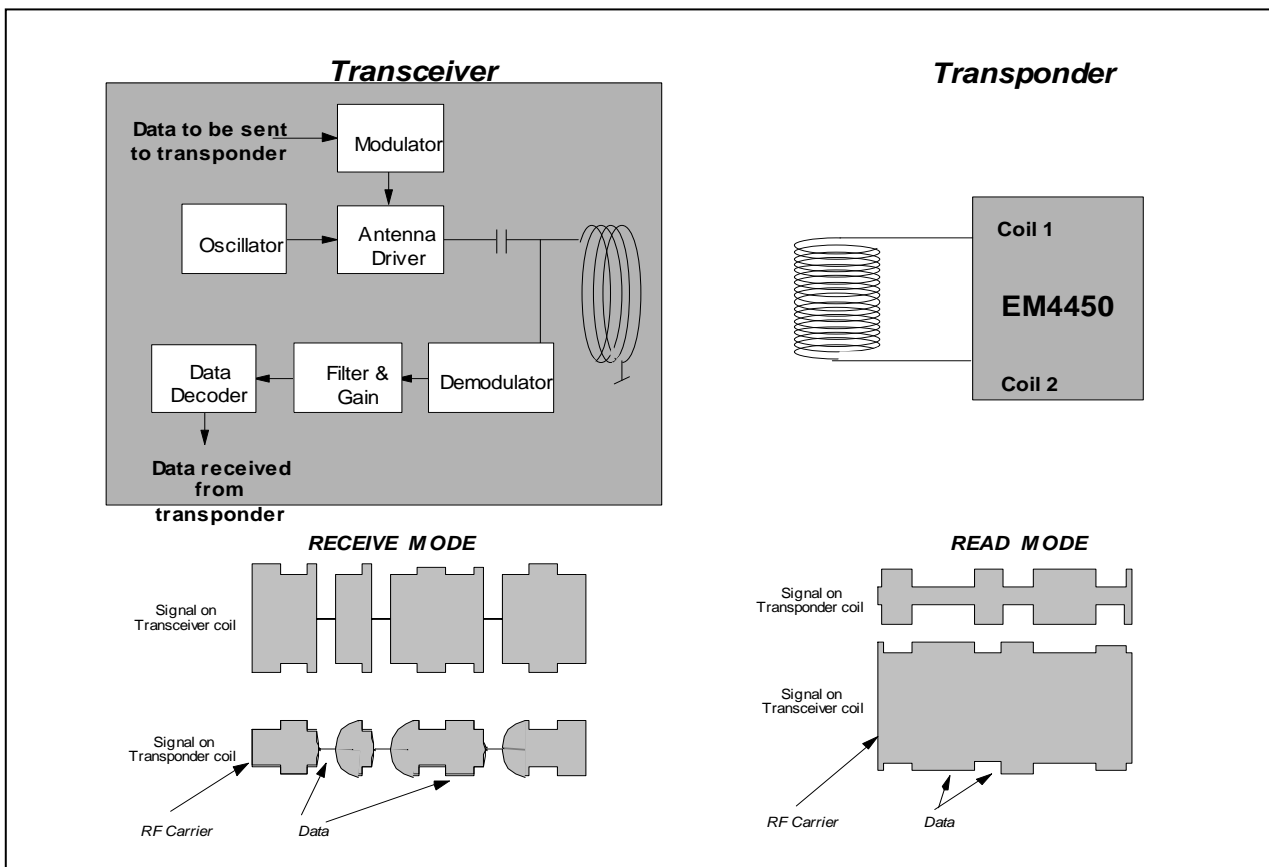
Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak Current induced on COIL1 and COIL2	I_{COIL}	± 30 mA
Power Supply	V_{DD}	-0.3 to 3.5 V
Maximum Voltage other pads	V_{max}	V_{DD}+0.3V
Minimum Voltage other pads	V_{min}	V_{SS}-0.3V
Storage temperature	T_{store}	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	2000V

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_{op}	-40	+85	°C
Maximum coil current	I_{COIL}		10	mA
AC Voltage on Coil	V_{coil}		note 1	V_{pp}
Supply Frequency	f_{coil}	100	150	kHz

note 1: Maximum voltage is defined by forcing 10mA on Coil1 - Coil2.

Electrical Characteristics

V_{DD} =2.5V, V_{SS} =0V , f_{coil} = 125 kHz Sine wave , V_{coil} = 1V_{pp} , T_{op} = 25°C ,   unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.3		3.5	V
Minimum EEPROM write voltage	V_{DDee}		2			V
Power Check EEPROM write	$I_{PWcheck}$	V_{DD} = 2.8V			40	μA
Supply current / read	I_{rd}	Read Mode			3	μA
Suppy current / write	I_{wr}	Write mode (V_{DD} = 2.8V)			22	μA
Modulator ON voltage drop	V_{ON}	$V_{(COIL1 - VSS)}$ & $V_{(COIL2 - VSS)}$ I_{coil} = 100μA $V_{(COIL1 - VSS)}$ & $V_{(COIL2 - VSS)}$ I_{coil} = 5 mA			0.50 2.50	V V
Monoflop	T_{mono}		35		85	μs
Resonance Capacitor	C_r		166.6	170	173.4	pF
Powercheck level	$V_{PWcheck}$		2		2.85	V
Power On Reset level high	V_{prh}	Rising Supply	1		1.6	V
Clock extractor input min. Clock extractor input max.	V_{clkmin} V_{clkmax}	Minimum Voltage for Clock Extraction Max. Voltage to detect modulation stop	0.25		25	V_{pp} mV_{pp}
EEPROM data endurance	N_{cy}	Erase all / Write all at V_{DD} = 3.5 V	100'000			cycles
EEPROM retention	T_{ret}	Top = 55°C after 100'000 cycles (note 2)	10			years

note 2: Based on 1000 hours at 150°C

www.emmicroelectronic.com

Timing Characteristics

V_{DD} =2.5V, V_{SS}=0V, f_{coil} = 125 kHz Sine wave, V_{coil} = 1V_{pp} , T_{op} = 25°C   unless otherwise specified

All timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Conditions	Value	Unit
Option : 64 clocks per bit	*Opt64*			
Read Bit Period	t_{rdb}		64	RF periods
LIW/ACK/NACK pattern duration	t_{patt}		320	RF periods
Read 1 Word Duration	t_{rdw}	including LIW	3200	RF periods
Processing Pause Time	t_{pp}		64	RF periods
Write Access Time	t_{wa}		64	RF periods
Initialization Time	t_{init}		2112	RF periods
EEPROM write time	t_{wee}	V_{DD} = 3V	3200	RF periods
Option : 32 clocks per bit	*Opt32*			
Read Bit Period	t_{rdb}		32	RF periods
LIW/ACK/NACK pattern duration	t_{patt}		160	RF periods
Read 1 Word Duration	t_{rdw}	including LIW	1600	RF periods
Processing Pause Time	t_{pp}		32	RF periods
Write Access Time	t_{wa}		32	RF periods
Initialization Time	t_{init}		1056	RF periods
EEPROM write time	t_{wee}	V_{DD} = 3V	2624	RF periods

RF periods represent periods of the carrier frequency emitted by the transceiver unit. For example, if 125 kHz is used :
The Read bit period (Opt64) would be : 1/125'000*64 = 512 µs, and the time to read 1 word : 1/125'000*3200 = 25.6 ms.
The Read bit period (Opt32) would be : 1/125'000*32 = 256 µs, and the time to read 1 word : 1/125'000*1600 = 12.8 ms.

ATTENTION
Due to amplitude modulation of the coil-signal, the clock-extractor may miss clocks or add spurious clocks close to the edges of the RF-envelope. This desynchronisation will not be larger than ±3 clocks per bit and must be taken into account when developing reader software.

Functional Description

General
The EM4450 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the DC voltage crosses the Power-On level, the chip enters the Standard Read Mode and sends data continuously. The data to be sent in this mode is user defined by storing the first and last addresses to be output. When the last address is sent, the chip will continue with the first address until the transceiver sends a request. In the read mode, a Listen Window (LIW) is generated before each word. During this time, the EM4450 will turn to the Receive Mode (RM) if it receives a valid RM pattern. The chip then expects a valid command.
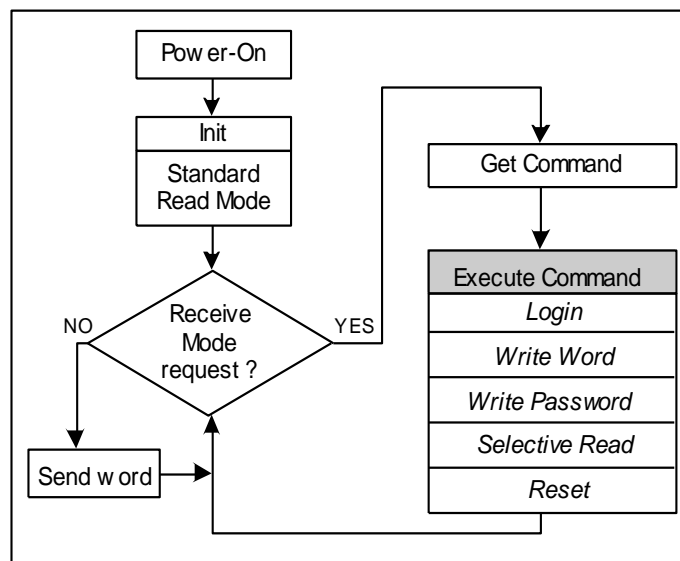
Mode of Operation

Fig. 4

www.emmicroelectronic.com

Memory Organisation

The 1024 bit EEPROM is organised in 32 words of 32 bits. The first three words are assigned to the Password, the Protection word, and the Control word. In order to write one of these three words, it is necessary to send the valid password. At fabrication, the EM4450 comes with all bits of the password programmed to a logic "0". The Password cannot be read out. The memory contains two extra words of Laser ROM. These words are laser programmed during fabrication for every chip, are unique and cannot be altered.
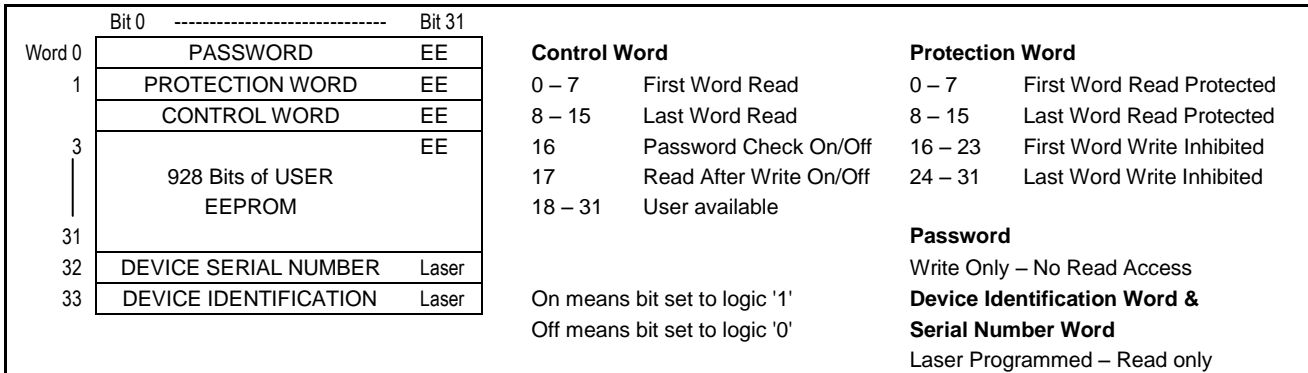
Memory Map

	Bit 0 ----------------------------- Bit 31		**Control Word**		**Protection Word**	
Word 0	PASSWORD	EE	0 – 7	First Word Read	0 – 7	First Word Read Protected
1	PROTECTION WORD	EE	8 – 15	Last Word Read	8 – 15	Last Word Read Protected
	CONTROL WORD	EE	16	Password Check On/Off	16 – 23	First Word Write Inhibited
3		EE	17	Read After Write On/Off	24 – 31	Last Word Write Inhibited
	928 Bits of USER		18 – 31	User available		
	EEPROM				**Password**	
31					Write Only – No Read Access	
32	DEVICE SERIAL NUMBER	Laser			**Device Identification Word &**	
33	DEVICE IDENTIFICATION	Laser	On means bit set to logic '1'		**Serial Number Word**	
			Off means bit set to logic '0'		Laser Programmed – Read only	

Fig.5

Standard Read Mode

After a Power-On-Reset and upon completion of a command, the chip will execute the Standard Read Mode, in which it will send data continuously, word by word from the memory section defined between the First Word Read (FWR) and Last Word Read (LWR). When the last word is output, the chip will continue with the first word until the transceiver sends a request. If FWR and LWR are the same, the same word will be sent repetitively. The Listen Window (LIW) is generated before each word to check if the transceiver is sending data. The LIW has a duration of 320 (160 opt 32) periods of the RF field. FWR and LWR have to be programmed as valid addresses (FWR $\leq$ LWR and $\leq$ 33).

The words sent by the EM4450 comprise 32 data bits and parity bits. The parity bits are not stored in the EEPROM, but generated while the message is sent as described below. The parity is even for rows and columns, meaning that the total number of "1's" is even (including the parity bit).
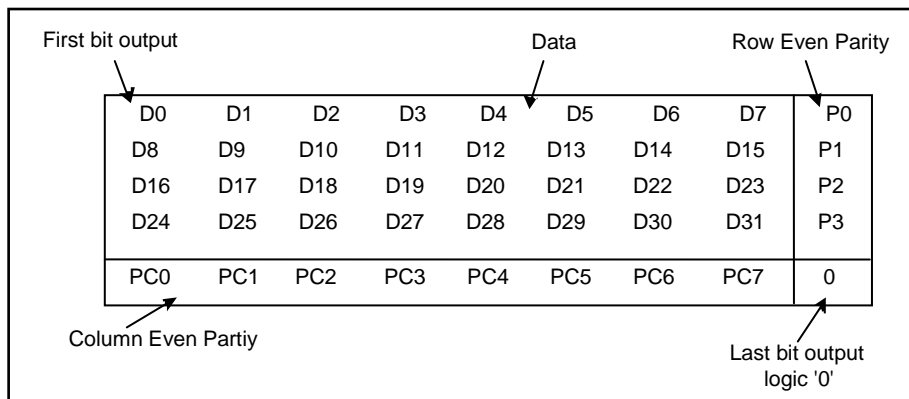
Word organisation (Words 0 to 33)

First bit output				Data			Row Even Parity	
D0	D1	D2	D3	D4	D5	D6	D7	P0
D8	D9	D10	D11	D12	D13	D14	D15	P1
D16	D17	D18	D19	D20	D21	D22	D23	P2
D24	D25	D26	D27	D28	D29	D30	D31	P3
PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7	0

Column Even Partiy

Last bit output logic '0'

Fig. 6

When a word is read protected, the output will consist of 45 bits set to logic "0". The password has to be used to output correctly a read protected memory area.
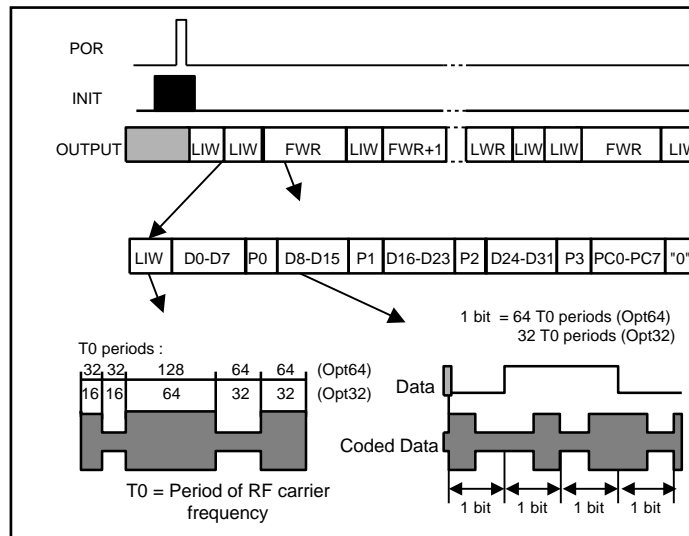
Read Sequence

Fig. 7

Receive Mode

To activate the Receive Mode, the Transceiver sends to the chip the RM pattern (while in the modulated phase of a Listen Window LIW). The EM4450 will stop sending data upon reception of a valid RM. The chip then expects a command. The RM pattern consists of 2 bits "0" sent by the transceiver. The first bit "0" transmitted is to be detected during the 64 (32 opt 32) periods where the modulation is "ON" in LIW.
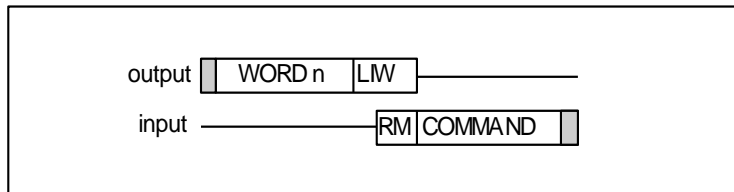

Fig. 8

Commands

The commands are composed of nine bits : eight data bits and one even parity bit (total amount of "ones" is even including the parity bit).

COMMAND BITS	FUNCTION
0 0 0 0 0 0 0 1 1	LOGIN
0 0 0 1 0 0 0 1 0	WRITE PASSWORD
0 0 0 1 0 0 1 0 0	WRITE WORD
0 0 0 0 1 0 1 0 0	SELECTIVE READ MODE
1 0 0 0 0 0 0 0 1	RESET

First bit Received   Parity bit

Fig. 9

Selective Read Mode

The Selective Read Mode is used to read other data than that defined between FWR and LWR. To enter Selective Read Mode, the Transceiver has to send during LIW a Receive mode pattern (RM) to turn the EM4450 in Receive Mode. Then the Selective Read Mode Command is sent by the transceiver followed by the First and Last addresses to be read. The FWR and LWR are then replaced by the new addresses and the chip is operating in the same way as the Standard Read Mode. The control word is not modified by this command, and the next standard read mode operation will work with original FWR and LWR (Selected area is read once and then the chip returns to Standard Read Mode).

To read words which are Read Protected, a Login command has to be sent by the transceiver prior to the Selective Read command. The Login command is to be used only once for all subsequent commands requiring a password.

The Selective Read mode command is followed by a single 32-bit word containing the new first and last addresses. Bits 0 to 7 correspond to the First Word Read and bits 8 to 15 correspond to the Last Word Read. Bits 16 to 31 have to be sent but are not used in the chip. The parities must be sent according to the word organisation as described in fig.7. Note that bit 31 is transmitted first.

To read the device Identification or the Serial Number, the Selective Read Command allows direct access to the Laser programmed words. These words can also be addressed in the standard read mode by selecting the addresses accordingly.
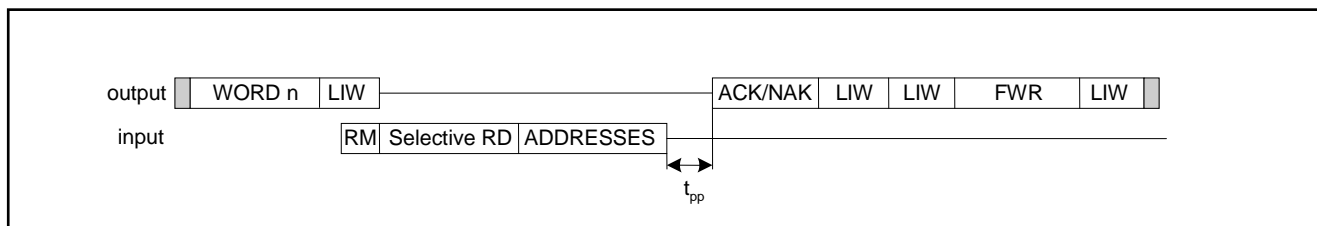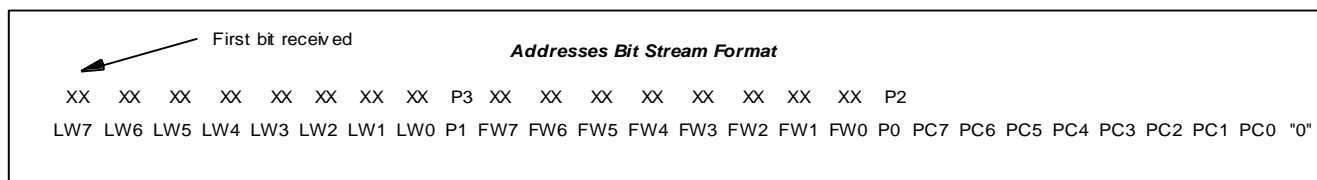

Fig. 10

Fig. 11

Reset Command

The Reset Command will return from any mode to the Standard Read Mode. The next word out is the FWR.
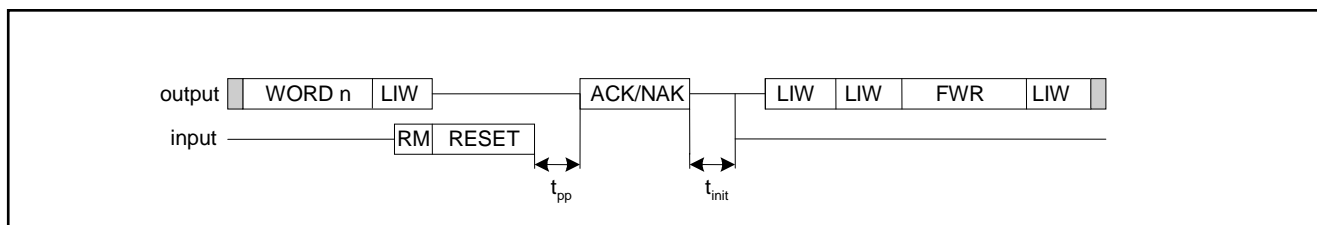

Fig. 12

Login

The Login command is used to access protected memory areas. This command has to be used only once to perform several password protected commands. The Power-On-Reset sequence and the Reset command will reset the password entry, and a new Login command has to be received to perform further password protected operations.

Upon reception of a correct password, the EM4450 will respond with an acknowledge pattern (ACK) and then continue in Standard Read Mode. If the Login is correct then password protected operations are allowed. If the password is incorrect, a NAK pattern is issued and password protected operations will not be possible (refer to Write Word for password data structure).
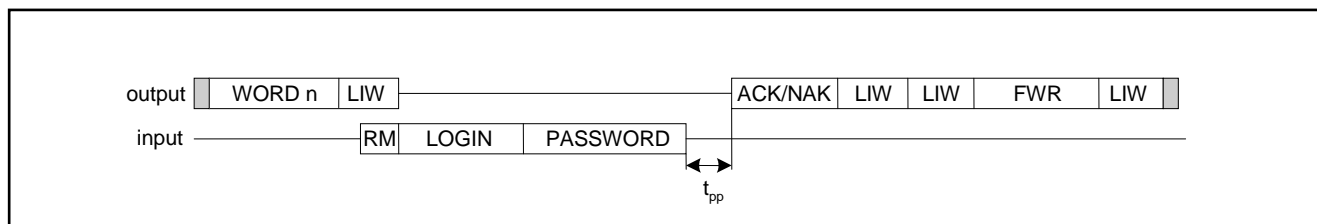

Fig. 13

If bit 16 of the control word is disabled (Password Check ON/OFF), the Login is still mandatory to modify the Protection Word, the Control Word, and the Password, but not to write in the EEPROM which is not write inhibited. In order to modify a write inhibited word, the Protection word has to be modified first. The Read protected area always requires the Login to be read. If the Write Protection Word is write protected, the write protection configuration is locked.

Write Password

When a Write Password command is received, the chip next expects information on the actual valid password. The chip sends back an ACK pattern if the password is correct. Then the chip expects the new password consisting of 32 bits + parity bit to be stored in the EEPROM. The chip will respond with an ACK pattern for a correct reception of data upon reception of the new password, and then will send another acknowledge pattern (ACK) to announce that the data is stored in the EEPROM. The Read after Write function has no effect on this command. If the password is wrong or the transmission is faulty, the chip will : send a NAK pattern; return to the Standard Read Mode; and, the password will remain the same. (Refer to Write Word for password data structure).
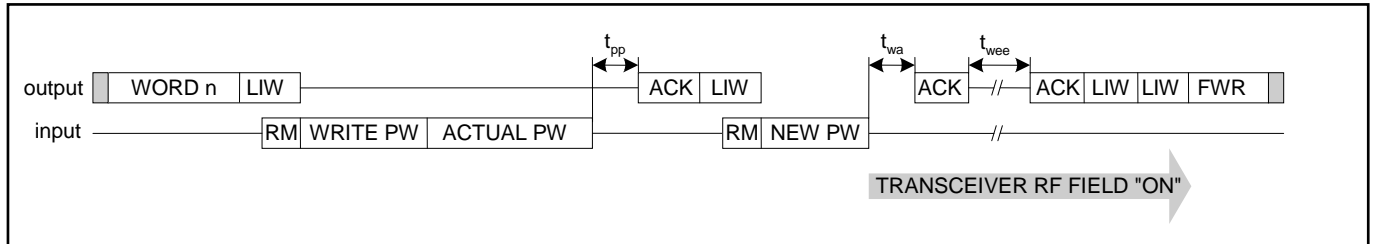

Fig. 14

Write Word

The Write mode allows modification of the EEPROM contents word by word. To modify address 1 (Protection word) and address 2 (Control word), it is mandatory to first send a Login command in order to Log in (like in a computer). The new written values will take effect only after performing a Reset command. It is strongly recommended to check the result of modifying the contents of these addresses effecting the function of the chip. Address 0 (Password) cannot be modified with this command but can be changed with the Write Password command.

Addresses 3 to 31 are programmable according to the defined protections. If the Password Check bit is off (bit 16 of control word) and the word is not write inhibited, the selected word can be freely modified without password. If the Password Check bit is on and the word is not write inhibited, the selected word can be modified with a previous Login. In any case, if the word is write inhibited, the protection word has to be changed before programming can occur.

Write to Address	Check Password bit (bit 16 / Control word)	Write Inhibit (Protection word)	Write Operation
0	X	X	Only with Write Password command
1 – 2	X	OFF	Login always required
1 – 2	X	ON	Write configuration LOCKED
3 – 31	OFF	OFF	Freely programmable
3 – 31	ON	OFF	Login required
3 – 31	X	ON	Change protection word first

The Write Word command is followed by the address and data. The address consists of a 9 bit block containing 8 data bits and 1 even parity bit. Only 6 bits from the data section are used for the word addressing, and the first three bits sent must be "0". The data consists of 4 times 9 bit blocks, each block consisting of 8 data bits and 1 associated even parity bit and one additional block consisting of 8 column parity bits and "0" as stop bit (Refer to fig. 7)
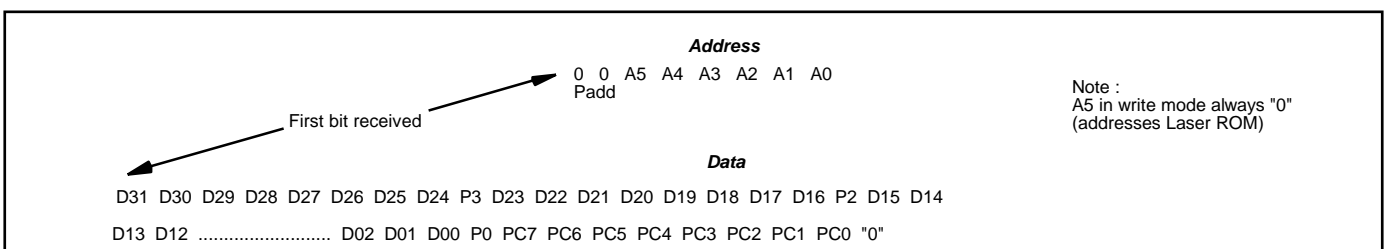

Fig. 15

After reception of the command, the address, and the data, the EM4450 will check the parity, the write protection status, the Login status, and also if the available power from the RF field is sufficient. If all the conditions are satisfied, an acknowledge pattern (ACK) will be issued afterward and the EEPROM writing process will start. At the end of programming, the chip will send an Acknowledge pattern (ACK). If at least one of the checks fails, the chip will issue a no acknowledge pattern (NAK) instead of ACK and return to the Standard Read Mode. The Transceiver will keep the RF field permanently "ON" during the whole writing process time.

The Read After Write function (bit 17 of Control word) controls the mode of operation following a write operation. When "ON" the latest written word will be read out and output next to the ACK pattern and two Listen Windows (LIW-LIW) even if the word is read protected. When "OFF", the ACK is followed immediately by a LIW-LIW and FWR. The last written word is not output.

If a request from the transceiver to return in receive mode (RM) is generated during the LIW, another word can be written in. Otherwise, the EM4450 will return in the Standard Read Mode.
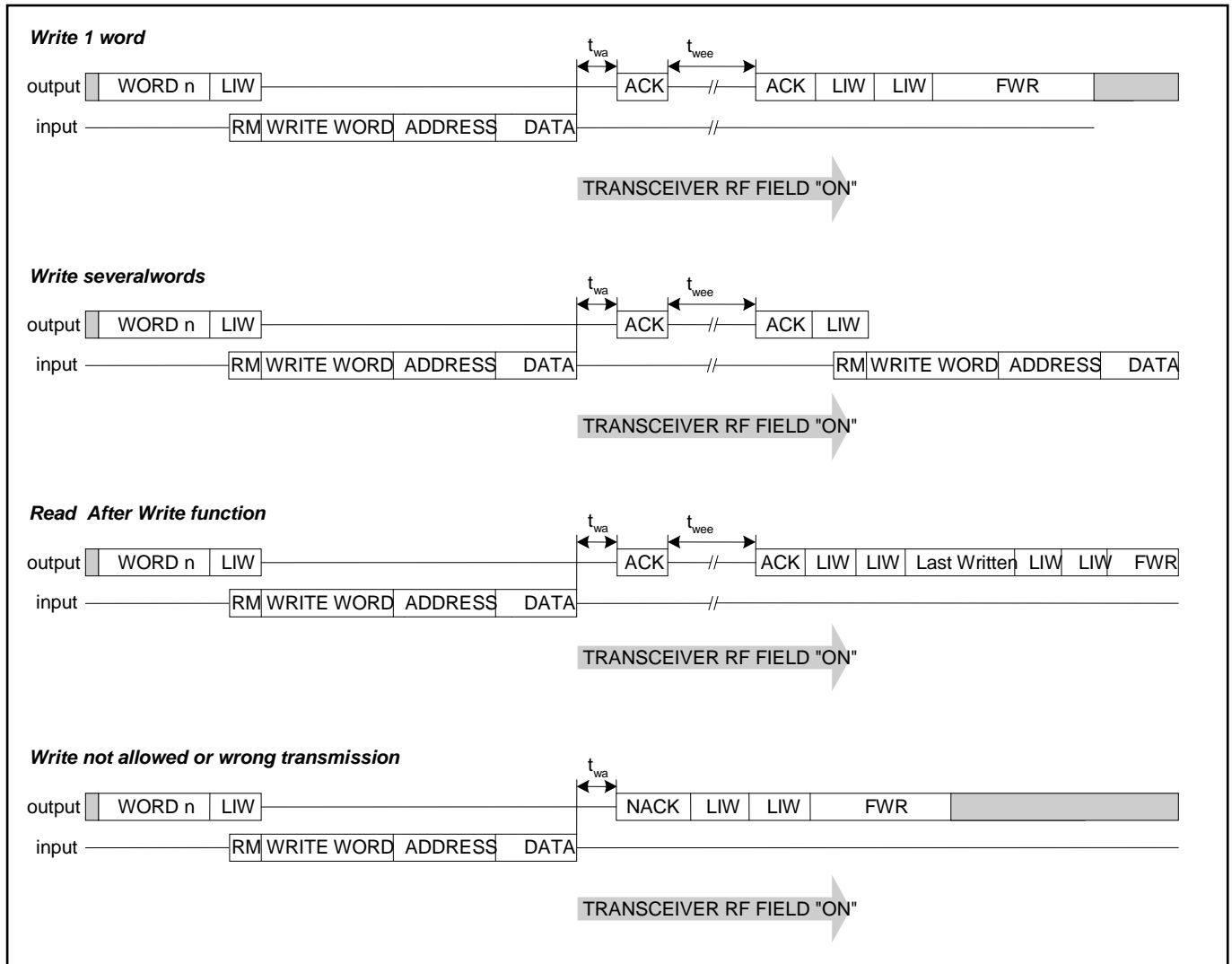

Fig. 16

Power-On-Reset (POR)

When the EM4450 with its attached coil enters an electromagnetic field, the built in AC/DC converter will supply the chip. The DC voltage is monitored and a Reset signal is generated to initialise the logic. The contents of the Control word and Protection word will be downloaded to enable the functions (INIT). The Power-On-Reset is also provided in order to make sure that the chip will start issuing correct data. Hysteresis is provided to avoid improper operation at the limit level.
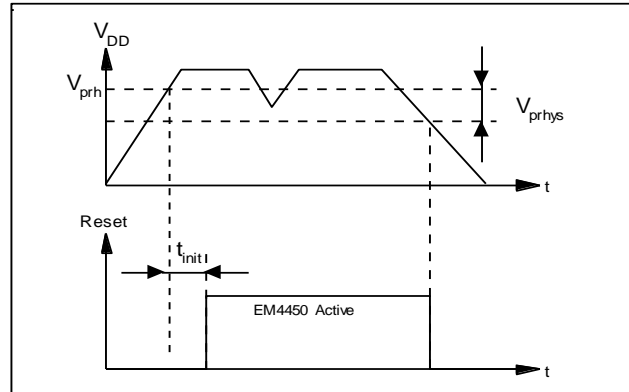

Fig. 17

Lock All / Lock Memory Area

The EM4450 can be converted to a Read Only chip or be configured to Read/Write and Read Only Areas by programming the protection word. This configuration can be locked by write inhibiting the Write Protection Word. Great care should be taken in doing this operation as there is no further possibility to change the Write Protection Word. The Control Word can also be protected in the same way thus freezing the operation mode.

Clock Extractor

The Clock extractor will generate a system clock with a frequency corresponding to the frequency of the RF field. The system clock is used by a sequencer to generate all internal timings.

Data Extractor

The transceiver generated field will be amplitude modulated to transmit data to the EM4450. The Data extractor demodulates the incoming signal to generate logic levels, and decodes the incoming data.

Modulator

The Data Modulator is driven by the serial data output from the memory which is Manchester encoded. The modulator will draw a large current from both coil terminals, thus amplitude modulating the RF field according to the memory data.

AC/DC Converter and Voltage Limiter

The AC/DC converter is fully integrated on chip and will extract the power from the incident RF field. The internal DC voltage will be clamped to avoid high internal DC voltage in strong RF fields.

Special Timings

The Processing Pause Time (t_{pp}), Write Access Time (t_{wa}) and EEPROM Write Time (t_{wee}) are timings where the EM4450 is executing internal operations. During these pauses, the RF field will be influenced.
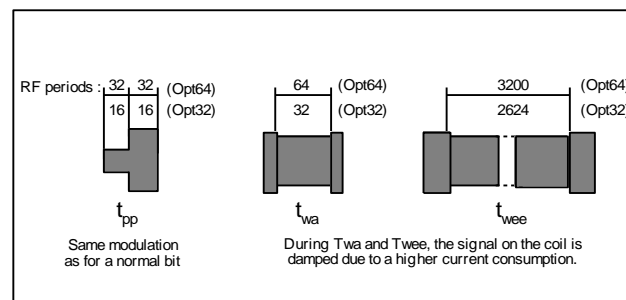

Fig. 18

Communication from Transponder to the Transceiver (READ MODE)

The EM4450 modulates the amplitude of the RF field to transmit data to the transceiver. Data are output serially from the EEPROM and Manchester encoded.
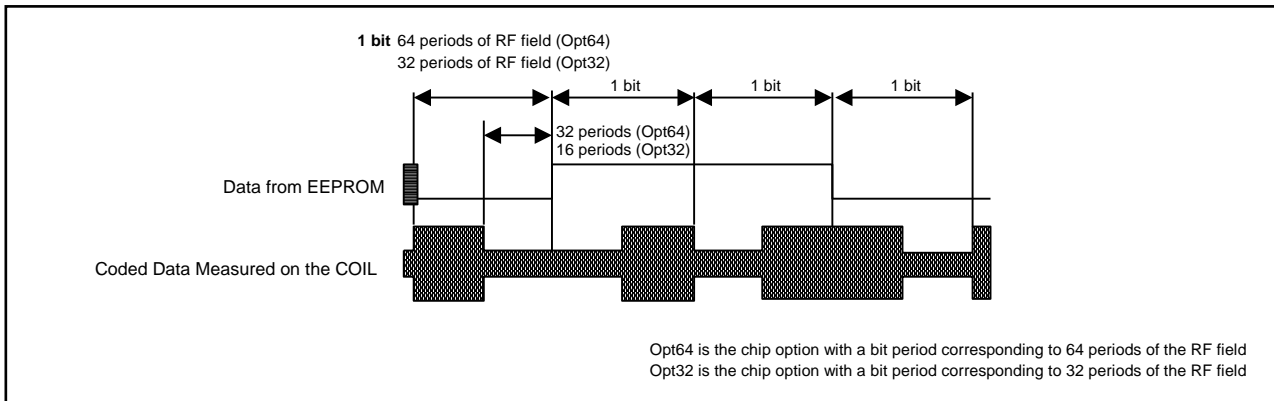
Fig. 19

The EM4450 uses different patterns to send status information to the transceiver. Their structure can not be confused with a bit pattern sequence. These patterns are the Listen Window (LIW) to inform the transceiver that data can be accepted, the Acknowledge (ACK) indicating proper communication and end of EEPROM write, and the No Acknowledge (NAK) when something is wrong.

The LIW, due to its special structure, can be used to synchronize the transceiver during a read operation. The LIW is sent before each word, and is sent twice before FWR.

All numbers represent number of periods of RF field

Opt64 is the chip option with a bit period corresponding to 64 periods of the RF field
Opt32 is the chip option with a bit period corresponding to 32 periods of the RF field
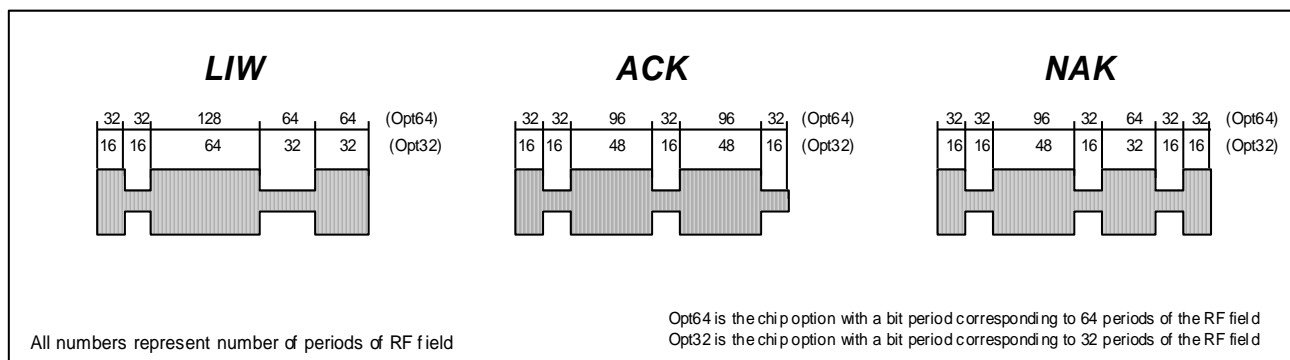
Fig. 20

Communication from the Transceiver to the Transponder (RECEIVE MODE)

The EM4450 can be switched to the Receive Mode ONLY DURING A LISTEN WINDOW. The Transceiver is synchronized with the incoming data from the transponder and expects a LIW before each word. During the phase where the chip has its modulator "ON" (64/32 periods of RF [Opt64/Opt32]), the transceiver has to send a bit "0". A certain phase shift in the read path of the transceiver can be accepted due to the fact that when entering Receive Mode, the Transceiver becomes the Master.

At reception of the first "0", the chip immediately stops the LIW sequence and then expects another bit "0" to activate the receive mode. Once the EM4450 has received the first bit "0", the transceiver is imposing the timing for synchronisation.

The EM4450 turns "ON" its modulator at the beginning of each frame of a bit period. To send a logic "1" bit, the transceiver continues to send clocks without modulation. After half a bit period, the modulation device of the EM4450 is turned "OFF" allowing recharge of the internal supply capacitor. To send a logic "0" bit, the transceiver stops sending clocks (100% modulation) during the first half of a bit period. The transceiver must not turn "OFF" the field after 7/4 clocks of the bit period (Opt64/Opt32). The field is stopped for the remaining first half of the bit period, and then turned "ON" again for the second half of the bit period. The 32rd/16th clock (Opt64/Opt32) defines the end of the bit.

To ensure synchronisation between the transceiver and the transponder, a logic bit set to "0" has to be transmitted at regular intervals. The RM pattern consists of two bits set to "0" thus allowing initial synchronisation. In addition, the chosen data structure contains even parity bits which will not allow more than eight consecutive bits set to logic "1" where no modulation occurs.

While the transceiver is sending data to the transponder, two different modulations will be observed on both coils. During the first half of the bit period, the EM4450 is switching "ON" its modulation device causing a modulation of the RF field. This modulation can also be observed on the transceiver's coil. The transceiver sending a bit "0" will switch "OFF" the field, causing a 100% modulation being observed on the transponder coil.
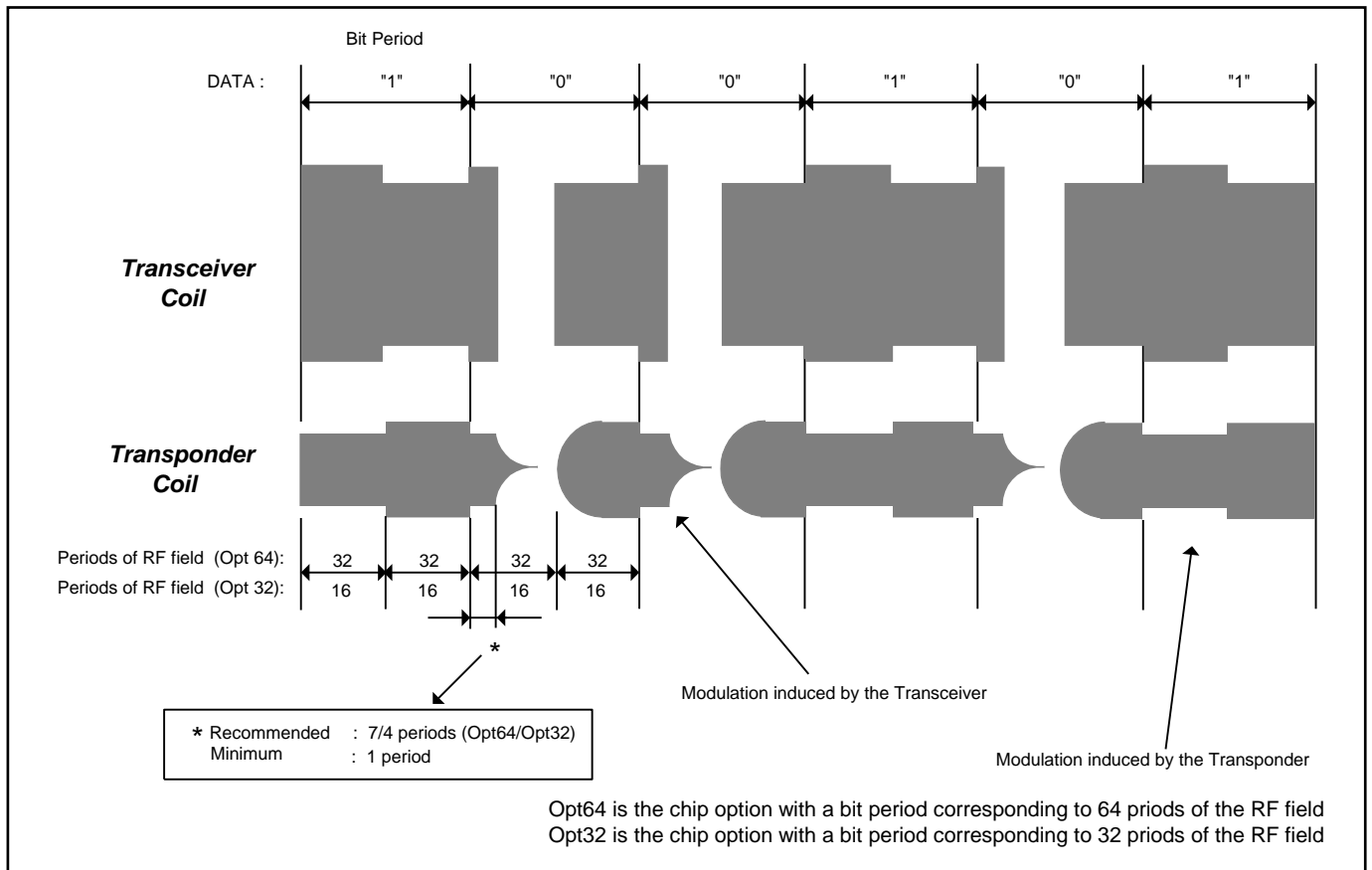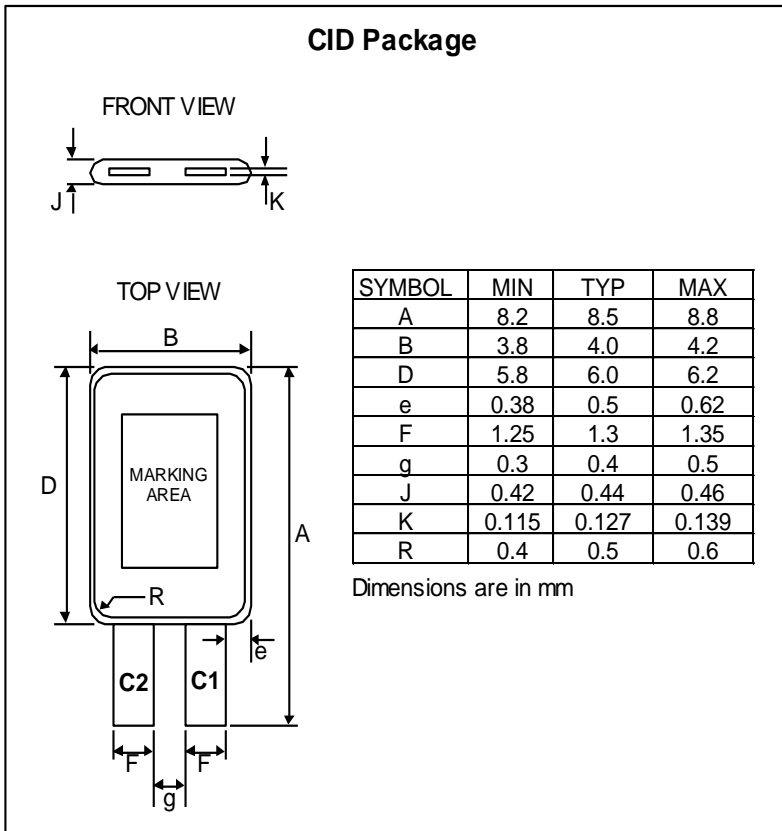
Fig. 21

www.emmicroelectronic.com

Package Information

Dimensions of PCB and CID version

CID Package

FRONT VIEW

J   K

TOP VIEW

B

D

MARKING
AREA

A

R

C2   C1

F   F

g

e

SYMBOL	MIN	TYP	MAX
A	8.2	8.5	8.8
B	3.8	4.0	4.2
D	5.8	6.0	6.2
e	0.38	0.5	0.62
F	1.25	1.3	1.35
g	0.3	0.4	0.5
J	0.42	0.44	0.46
K	0.115	0.127	0.139
R	0.4	0.5	0.6

Dimensions are in mm

Fig. 22

PCB Package

Y   Z

X

C2   C1

SYMBOL	MIN	TYP	MAX
X		8.0	
Y		4.0	
Z			1.0

Dimensions are in mm

Fig. 23

www.emmicroelectronic.com

Chip Floor Plan
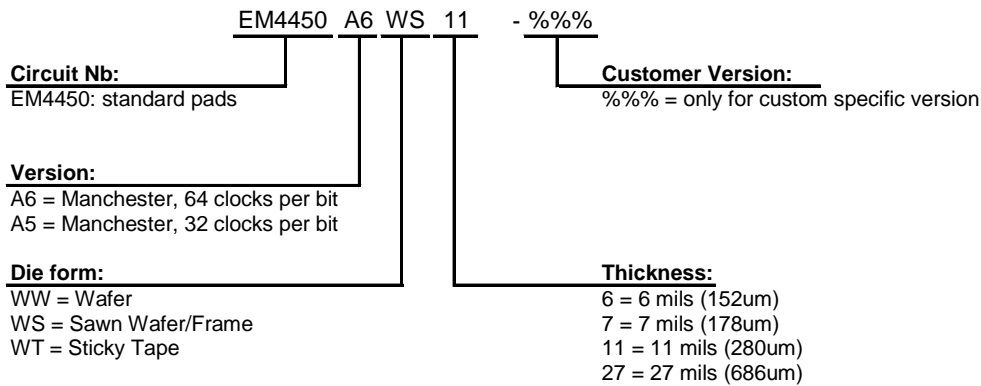

Pad size : 86 X 86   All dimensions in μm
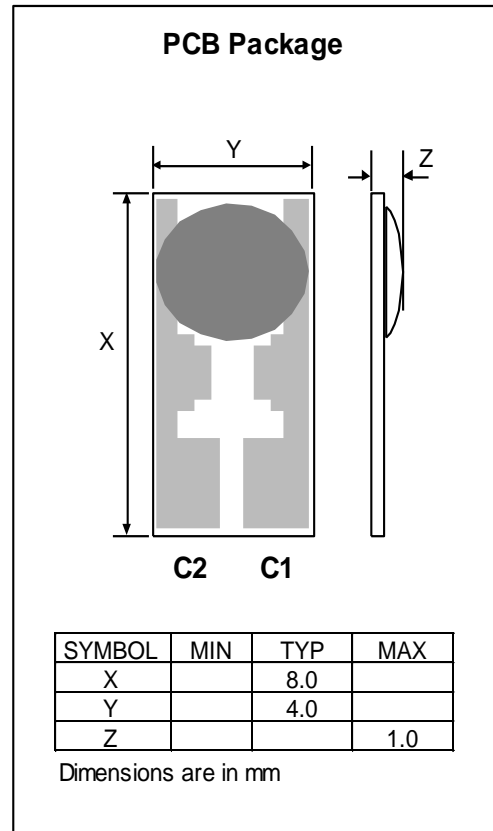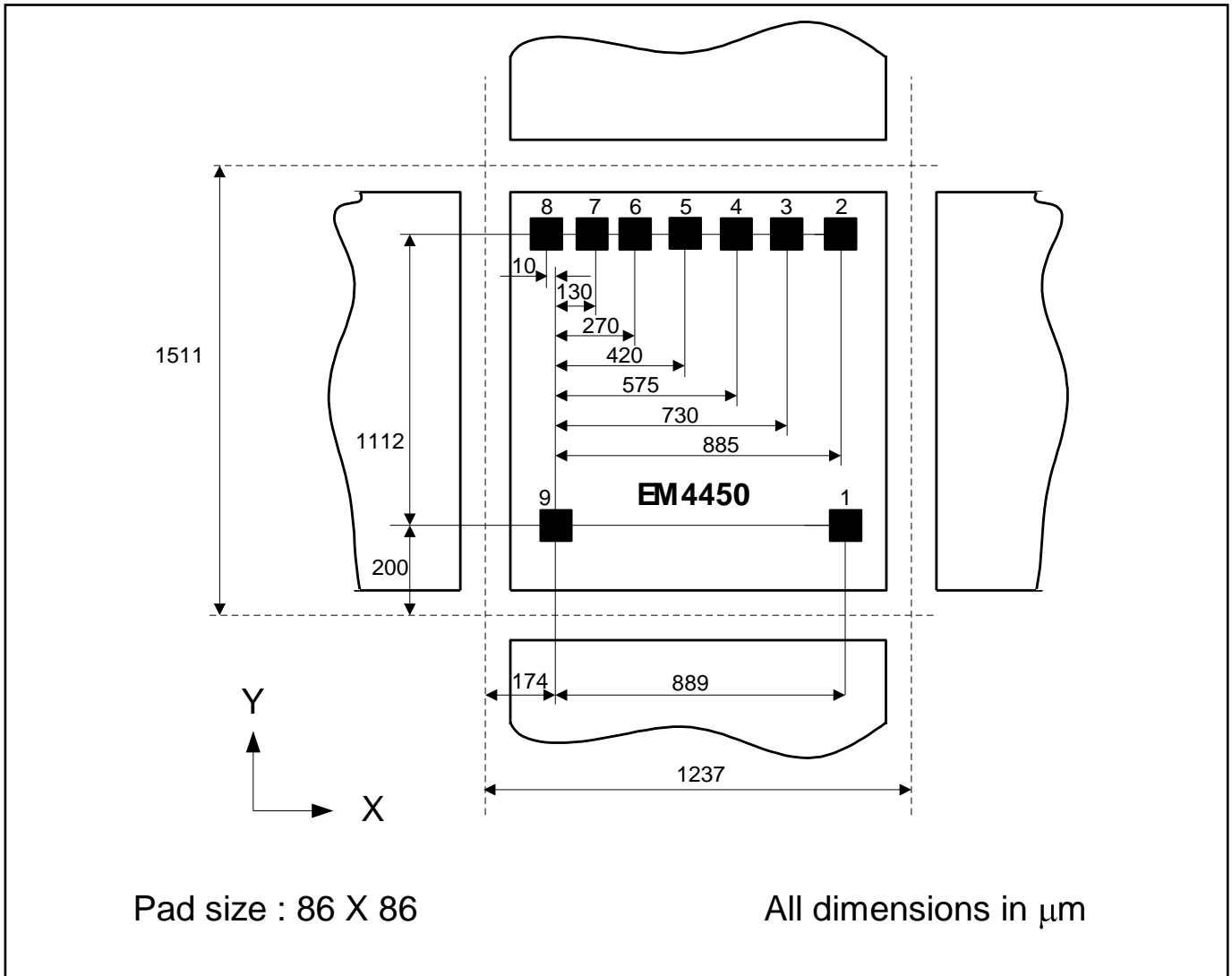
Fig. 24

Pad Description

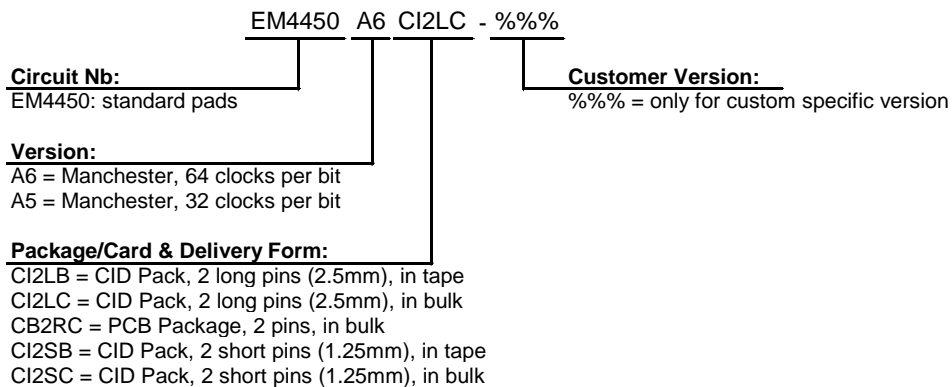| Pad	Name	Function
1	COIL1	Coil Terminal 1
2	TEST_CLK	Test Clock input with pull-down
3	TEST_IN	Test Input with pull-down
4	TEST	Test Mode Input with pull-down
5	TEST_OUT	Test Output
6	VDD	Positive Internal Supply Voltage
7	VPOS	Internal Supply
8	VSS	Negative Internal Supply Voltage
9	COIL2	Coil Terminal 2

Ordering Information

Die Form

This chart shows general offering; for detailed Part Number to order, please see the table "Standard Versions" below.

EM4450 A6 WS 11 - %%%

Circuit Nb:
EM4450: standard pads

Customer Version:
%%% = only for custom specific version

Version:
A6 = Manchester, 64 clocks per bit
A5 = Manchester, 32 clocks per bit

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WT = Sticky Tape

Thickness:
6 = 6 mils (152um)
7 = 7 mils (178um)
11 = 11 mils (280um)
27 = 27 mils (686um)

Packaged Devices

This chart shows general offering; for detailed Part Number to order, please see the table "Standard Versions" below.

EM4450 A6 CI2LC - %%%

Circuit Nb:
EM4450: standard pads

Customer Version:
%%% = only for custom specific version

Version:
A6 = Manchester, 64 clocks per bit
A5 = Manchester, 32 clocks per bit

Package/Card & Delivery Form:
CI2LB = CID Pack, 2 long pins (2.5mm), in tape
CI2LC = CID Pack, 2 long pins (2.5mm), in bulk
CB2RC = PCB Package, 2 pins, in bulk
CI2SB = CID Pack, 2 short pins (1.25mm), in tape
CI2SC = CID Pack, 2 short pins (1.25mm), in bulk

Remarks:
- For ordering please use table of "Standard Version" table below.
- For specifications of Delivery Form, including tape and bulk, as well as possible other delivery form or packages, please contact EM Microelectronic-Marin S.A.

Standard Versions & Samples:

For samples please order exclusively:

Part Number	Bit coding	Cycle/bit	Pads	Package	Delivery Form
EM4450 A6 CI2LC	Manchester	64	Standard	CID package, 2 pins (length 2.5mm)	bulk
EM4450 A6 CB2RC	Manchester	64	Standard	PCB Package, 2 pins	bulk

The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A. Please make sure to give complete part number when ordering, <u>without spaces between characters</u>.

Part Number	Bit coding	Cycle/bit	Pads	Package/Die Form	Delivery Form / Bumping
EM4450 A5 CB2RC	Manchester	32	Standard	PCB Package, 2 pins	bulk
EM4450 A5 CI2LC	Manchester	32	Standard	CID package, 2 pins (length 2.5mm)	bulk
EM4450 A6 CB2RC	Manchester	64	Standard	PCB Package, 2 pins	bulk
EM4450 A6 CI2LB	Manchester	64	Standard	CID package, 2 pins (length 2.5mm)	tape
EM4450 A6 CI2LC	Manchester	64	Standard	CID package, 2 pins (length 2.5mm)	bulk
EM4450 XX YYY-%%%	Manchester	32/64	Standard	custom	custom

Product Support

Check our Web Site under Products/RF Identification section.
Questions can be sent to cid@emmicroelectronic.com